xBGAS: An Address Space Extension for Scalable High Performance Computing

[1]Xi Wang, [2]John D. Leidel, [1]Brody Williams, [3]Alan Ehret, [3]Miguel Mark, [3]Sahan Bandara, [3]Michel Kinsy, [1]Yong Chen
[1]Texas Tech University, [2]Tactical Computing Laboratories, [3] Texas A&M University

1

Abstract

Given the recent reemergence of advanced memory and device interconnection technologies such as CCIX, GenZ and OpenCAPI, we have witnessed a resurgence in interest in extending local node addressing to remote devices and storage. This interest is especially prominent in the high performance computing and high performance analytics communities as the need to exploit high bandwidth, low latency messaging techniques is critical to constructing scalable, efficient computing platforms.

xBGAS, is designed as a bridge extension for the RISC-V ISA, that extends the base 32/64 bits addressing in RV32I and RV64I to 64/128 bits, respectively with an extended set of registers and instructions. The goal of this extents-based model is providing high-performance inter-node communications via highly efficient micro-architecture design and advanced scalable shared memory programming environments.

3

xBGAS Design

1. One-sided Communications

- Memory semantics remote data accesses
- Kernel bypassing and zero remote CPU involvement

2. Micro-architecture Support

- Extended architecture
- RISC-V ISA extensions

3. Extended Addressing Capability

- Global address space mapped to extended address bits
- Machine-level runtime support for scalable shared memory programming model.

2

Introduction

Given the recent reemergence of extended memory interconnection technologies such as GenZ [1], CCIX [2] and OpenCAPI [3], architects in high performance computing (HPC) and high performance analytics (HPA) have sought to exploit these interconnection methodologies for extended or partitioned addressing across device and system architectural domains. However, we have yet to see a commercial architecture with native extended addressing capabilities in the ISA garner wide adoption.

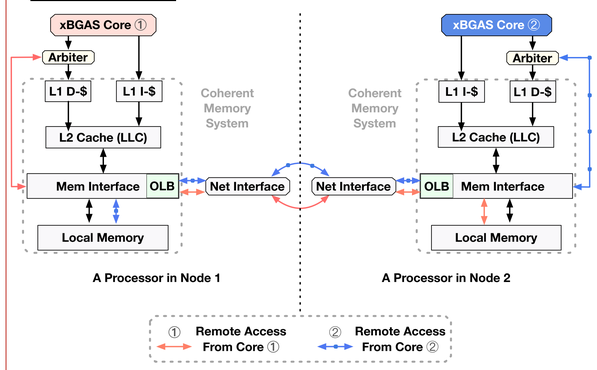
Therefore, the **Extended Base Global Address Space (xBGAS)** extension is introduced to provide extended addressing capabilities beyond the core 64-bit addressing modes in the base RISC-V RV64I ISA for HPC. The introduced extended memory models can be potentially utilized in the **HPC-PGAS, Security, Distributed file systems, HPC-FLAT, MMAP-IO, CloudBSP**, etc [4].

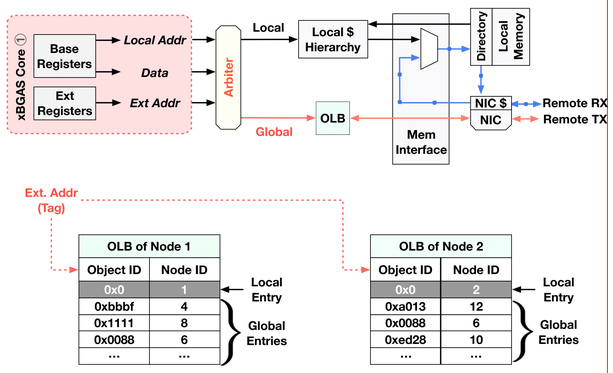
In this poster, we introduce the xBGAS extension in terms of:

- xBGAS architecture design
- ISA extension (xBGAS instructions, registers, etc.) [5]
- xBGAS software toolchains [7]
- Extended global address space
- Scalable shared memory management and runtime support [6]

4

Architecture





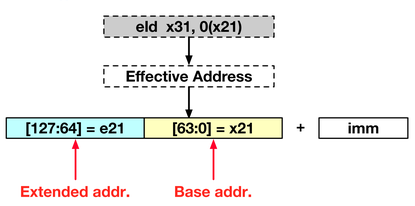
Arbiter arbitrates requests to the local memory system if extended address is 0. Otherwise, it is a remote reqeust

Object Lookaside Buffer (OLB) is a lookup table that maps shared data objects into extended addresses space

5

ISA Extension

Integer Load/Store Instructions



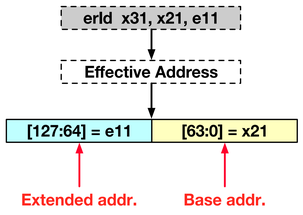
Load

```
eld  x31, 0(x21)
elw  x31, 0(x21)
elb  x31, 0(x21)
.......
```

Store

```
esd  x31, 0(x21)
esw  x31, 0(x21)
esb  x31, 0(x21)
.......
```

Raw Integer Load/Store Instructions



Raw Load

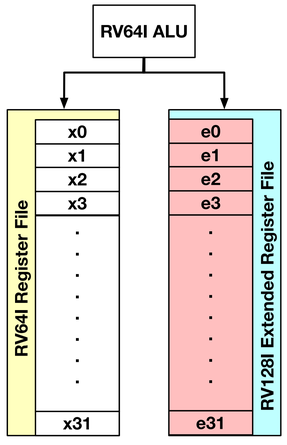
```
ersd  x31, x21, e11
ersw  x31, x21, e11
ersb  x31, x21, e11
.......
```

Raw Store

```
erld  x31, x21, e11
erlw  x31, x21, e11
erlb  x31, x21, e11
.......
```

6

Register Extensions



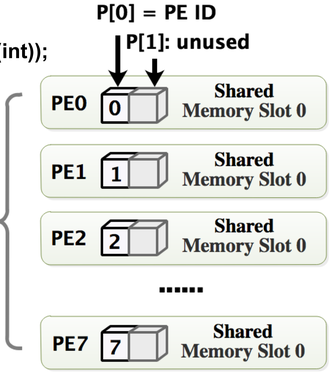
- 32 Extended Registers: e0 ~ e31 [4].

7

Symmetric Shared Memory Management

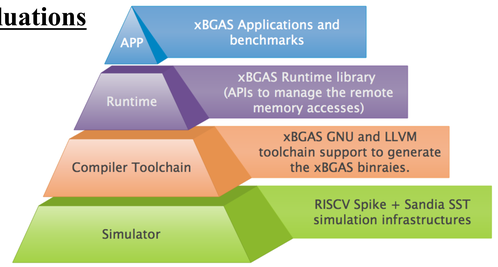
```
/* Shared memory allocation */
int *p = (int*)xbrtime_malloc(2*sizeof(int));

/* Set p[0] = My PE ID*/
p[0] = xbrtime_mype();
```

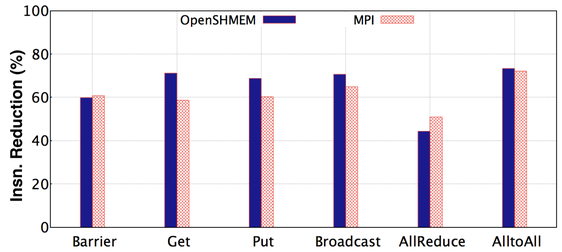
Distributed shared memory are symmetrically allocated

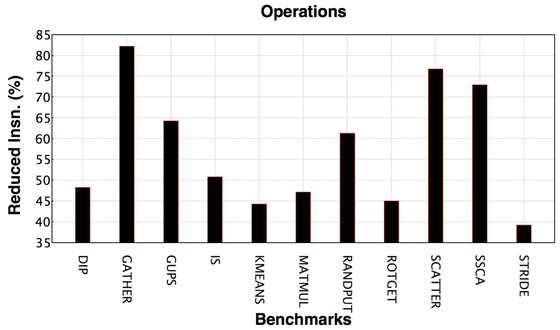


8

Evaluations







8

References:

[1] GenZ Consortium, "GenZ Core Specification", Tech Rep,. July 2017 http://genzconsortium.org/specifications/draft-core-specification- july-2017/
[2] "CCIX Consortium," https://www.ccixconsortium.com/, accessed: 2017-09-09.
[3] "OpenCAPI Consortium," http://opencapi.org/, accessed: 2017-09-09.
[4] John D. Leidel, David Donofrio, Fatollahi-Fard, Kurt Keville, xBGAS: A Bridge Proposal for RV128 and HPC, 7th RISC-V Workshop.
[5] xBGAS ISA spec, https://github.com/tactcomplabs/xbgas-archspec
[6] xBGAS Runtime, https://github.com/tactcomplabs/xbgas-runtime
[7] xBGAS Toolchain, https://github.com/tactcomplabs/xbgas-tools

TEXAS TECH UNIVERSITY · Tactical Computing Labs · Massachusetts Institute of Technology · BERKELEY LAB · TEXAS A&M UNIVERSITY